BANK 0

Block 0 — 111
Block 15 — 112
Total of 16
OOOOOOOO OOOOOOOO

Block 1
Block 0 — 110

BANK 1

Block 0
Block 15
Total of 16
OOOOOOOO OOOOOOOO

Block 1
Block 0

Global Bit Line

Total of 16
OOOOO OOOOO
en.0.15 — 122
en.0.0 — 121
en.0.8 — 120

Total of 16
OOOOO OOOOO
en.1.15
en.1.1
en.1.8

Total of 16
OOOOO OOOOO
en.2.15
en.2.1
en.2.0

Total of 16
OOOOO OOOOO
en.3.15
en.3.1
en.3.0

115
116
117
118

Reset

BANK 2
Blocks 0-15 — 107
Blocks 0-15

BANK 3
Blocks 0-15 — 108

we
blad_enble

105
108 — 138

Data Latch 0 — 135
Data Latch 1 — 136
Data Latch 15 — 137
130
131
132

Total of 16
0
0

BL driver 0 — 138
BL driver 1 — 139
BL driver 15 — 140

106

100

FIG. 1

FIG. 2

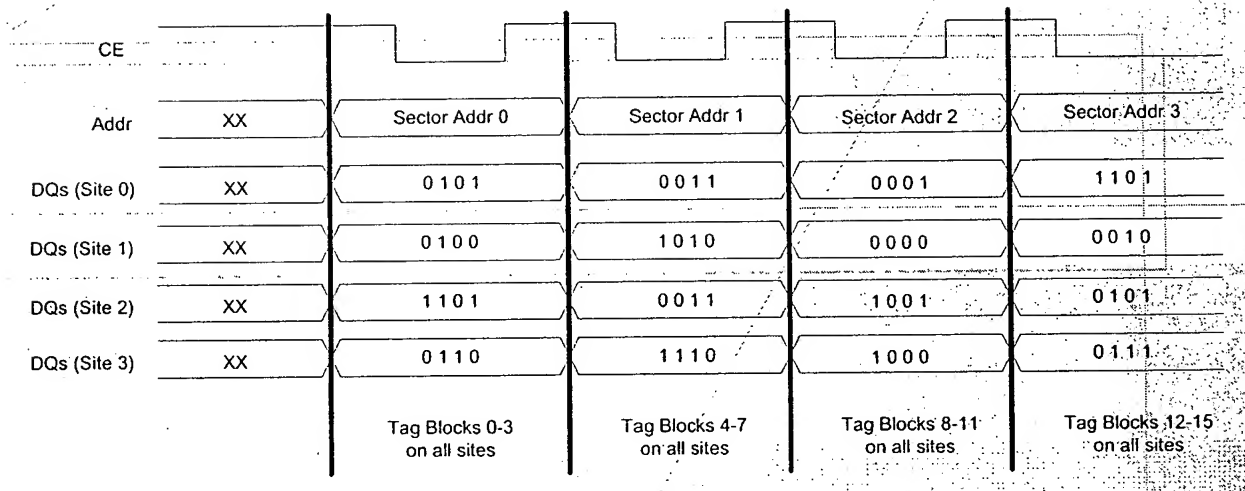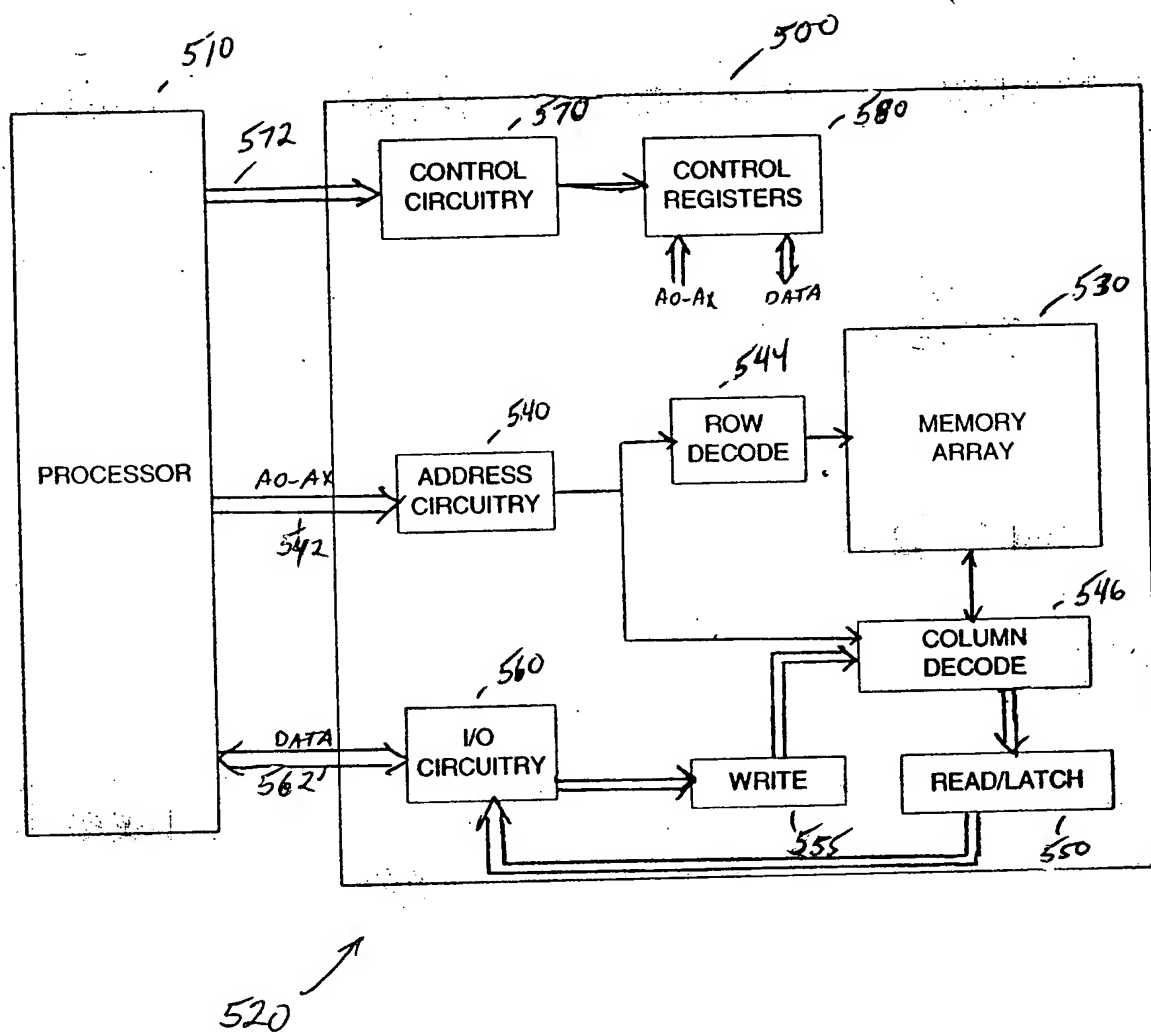| Sector Address Vector	DQ Vector			
	DUT0	DUT1	DUT2	DUT3
Sector Addr 0 (Blocks 0-3)	0 1 0 1	0 1 0 0	1 1 0 1	0 1 1 0
Sector Addr 1 (Blocks 4-7)	0 0 1 1	1 0 1 0	0 0 1 1	1 1 1 0
Sector Addr 2 (Blocks 8-11)	0 0 0 1	0 0 0 0	1 0 0 1	1 0 0 0
Sector Addr 3 (Blocks 12-15)	1 1 0 1	0 0 1 0	0 1 0 1	0 1 1 1

FIG. 3.

CE				
Addr	XX	Sector Addr 0	Sector Addr 1	Sector Addr 2	Sector Addr 3
DQs (Site 0)	XX	0 1 0 1	0 0 1 1	0 0 0 1	1 1 0 1
DQs (Site 1)	XX	0 1 0 0	1 0 1 0	0 0 0 0	0 0 1 0
DQs (Site 2)	XX	1 1 0 1	0 0 1 1	1 0 0 1	0 1 0 1
DQs (Site 3)	XX	0 1 1 0	1 1 1 0	1 0 0 0	0 1 1 1
		Tag Blocks 0-3 on all sites	Tag Blocks 4-7 on all sites	Tag Blocks 8-11 on all sites	Tag Blocks 12-15 on all sites

FIG. 4

FIG. 5